

SPECIFICATION OF
USSN 60/681,821

MATERIALS ISSUES OF NI FULLY SILICIDED (FUSI) GATES FOR CMOS APPLICATIONS

J. A. Kittl^{2*}, A. Lauwers¹, M. A. Pawlak¹, C. Demeurisse¹, K. G. Anil¹,
A. Veloso¹, M. J. H. van Dal³, T. Schram¹, B. Brijs¹, M. Kaiser³, S. Kubicek¹,
J. Cunniffe¹, R. Verbeeck¹, C. Vrancken¹, S. Biesemans¹ and K. Maex¹

¹ IMEC, Kapeldreef 75, B-3001, Leuven, Belgium

² Affiliate researcher at IMEC from Texas Instruments, Leuven, Belgium

³ Philips Research Leuven, Kapeldreef 75, B-3001, Leuven, Belgium

The Ni-silicide phases and morphology in Ni fully silicided gates were investigated for varying deposited Ni to Si thickness ratios and rapid thermal processing conditions. The presence of NiSi₂, NiSi, Ni₃Si₂, Ni₂Si, Ni₃₁Si₁₂ and Ni₃Si as predominant phases was observed for increasing Ni to Si thickness ratios. In most samples typically two of these phases were detected by X-ray diffraction. No secondary phases were detected on Ni₃Si samples (Ni/Si thickness ratio ~1.7). For samples targeting NiSi as gate electrode, RBS and TEM analysis confirmed a layered structure with NiSi at the interface and a Ni-rich silicide layer (Ni₂Si, Ni₃Si₂) on top. Process conditions were determined for formation of gate electrodes for NiSi, Ni₂Si and Ni₃Si. Only small changes in flat-band voltage or work function were found between these phases on SiO₂ or SiON for undoped samples. While significant changes in work function with dopants were observed for NiSi on SiO₂, little or no effects were found for NiSi on HfSiON (suggesting Fermi-level pinning) and for Ni₂Si on SiO₂. An increase of > 300 mV was found from NiSi to Ni₃Si on HfSiON, suggesting unpinning of the Fermi-level with the Ni-rich silicide.

INTRODUCTION

Metal gates are expected to replace partially silicided poly-Si gates in future complementary metal-oxide-semiconductor (CMOS) technology nodes, in order to eliminate poly-Si depletion issues. For this application, the work function (WF) is one of the most critical properties to be considered. Recently, there has been significant interest on the application of silicides as metal gate electrodes, and in particular, on NiSi fully-silicided (FUSI) gates [1-4]. From a processing point of view, it can be implemented as a variation of the Ni self-aligned silicidation process used in previous nodes in which the silicide is formed in the gate down to the dielectric interface, fully consuming the poly-Si film. Ni-silicide appears as an attractive metal gate candidate that allows maintaining several aspects of the flows from previous generations (such as Si gate pattern and etch, and self-aligned silicide processes). A key property that has attracted attention to NiSi FUSI gates is the modulation of their effective work function on SiO₂ by dopants [1-3],

* Contact Author: e-mail: kittlj@imec.be, phone: +32 16 28 1491

which may allow for tuning of the threshold voltage (V_t) of NMOS and PMOS devices without the need for two different metals. The integration and properties of Ni FUSI gates on high-k dielectrics is also of interest for advanced CMOS applications [4].

5 Good control of the WF and V_t of devices is an essential requirement for gate electrode applications. In order to assess the ability to control V_t for Ni FUSI gate processes and given the large number of silicide phases in the Ni-Si system [5], it is important to address a) the ability to control the Ni-silicide phase at the dielectric interface, and b) the work functions of different silicide phases (both for conventional and for high-K dielectrics). A study of these key materials issues is presented in this work.

10

EXPERIMENTS

Ni/poly-Si/dielectric stacks were deposited on (100) Si wafers, for varying film thicknesses, in the 30-170 nm and 60-100 nm ranges for Ni and Si films respectively. Dielectric films used in this study included SiO_2 , SiON , HfSiON and HfSiON/SiO_2 stacks of varying thicknesses with equivalent oxide thickness (EOT) in the 1-20 nm range.
15 Samples were reacted by rapid thermal processing (RTP) to form silicide films at temperatures in the 280-850 °C range, typically for 30 to 60 s. A wet etch used in self-aligned Ni-silicide processes (diluted sulfuric-peroxide solution) was subsequently performed. In some samples a second RTP anneal step was performed after the selective etch. Samples were characterized by X-ray diffraction (XRD) using Cu-K_α radiation,
20 transmission electron microscopy (TEM), scanning electron microscopy (SEM) and Rutherford backscattering spectrometry (RBS). Patterned fully silicided gate devices were also fabricated for electrical characterization, using a chemical-mechanical polishing (CMP) flow as described in reference [4] or a conventional flow (the latter used only for fabrication of capacitors overlapping isolation). Ion implantation was performed on
25 selected samples after poly-Si deposition, with some of these samples receiving an activation anneal.

RESULTS AND DISCUSSION

Ni-silicide phases in fully silicided gates

Several silicide phases can be formed in the Ni-Si system [5]. For the reaction of a
30 thin Ni film with a Si-substrate, Ni-rich phases form first at low temperatures [5, 6]. The presence of $\text{Ni}_{31}\text{Si}_{12}$ has been reported at early stages of the reaction, followed by formation of Ni_2Si [6]. Ni_2Si is generally the predominant phase at low temperatures and early stages of the reaction, forming a layer that grows by diffusion-limited kinetics [3, 5]. At higher temperatures and as Ni is consumed, NiSi nucleates and grows also by
35 diffusion-limited kinetics [3, 5]. The presence of Ni_3Si_2 has also been reported during early stages of the reaction [6], before nucleation of NiSi . The formation of the different Ni-rich silicide phases can also depend on film thickness and thermal history (ramp rates, etc.) during the reaction. As the reaction proceeds for the case of a Ni-film on a Si substrate, NiSi grows fully consuming the Ni-rich silicides. NiSi_2 nucleates and grows at
40 higher temperatures [3, 5, 6].

For Ni FUSI gate applications, deposited Ni films are reacted with either amorphous or polycrystalline Si films of limited thickness, deposited on top of a dielectric. The deposited Ni thickness to Si thickness ratio ($t_{\text{Ni}}/t_{\text{Si}}$) controls (in combination with the thermal history) the reacted Ni/Si ratio and phases obtained. It is essential for gate electrode applications that the silicide phase at the dielectric interface be well controlled, in order to ensure good control of the V_t of devices. The phases and morphology after full silicidation for varying $t_{\text{Ni}}/t_{\text{Si}}$ ratios and thermal processes were investigated, in order to assess and identify conditions for formation of gates with a controlled silicide phase at the dielectric interface. NiSi_2 films with NiSi as secondary phase (as determined by XRD) were obtained for $t_{\text{Ni}}/t_{\text{Si}} \sim 0.30\text{-}0.35$ at 800°C (Fig. 1). For applications in self-aligned silicide processes, the nucleation-controlled growth mechanism of NiSi_2 and its high nucleation temperature make it a less appealing candidate. If processing temperatures are kept below the nucleation temperature of NiSi_2 , a minimum $t_{\text{Ni}}/t_{\text{Si}}$ ratio of ~ 0.55 is required to allow full silicidation of the gate with NiSi . A larger $t_{\text{Ni}}/t_{\text{Si}}$ ratio (e.g. 0.6) is desirable, however, to ensure full silicidation and prevent the presence of Si grains at the dielectric interface, allowing for possible process variations in deposited film thickness. As a result, when targeting NiSi as gate electrode material, bi-layer silicide films are typically obtained with NiSi at the bottom and a Ni-rich silicide on top (Figs. 1 to 3). The thickness of each layer depends on the Ni/Si ratio, with a larger proportion of Ni-rich silicide as the ratio is increased (Figs. 1 and 2). The phases present in the upper Ni-rich silicide layer can depend on the Ni/Si ratio chosen and on the thermal history. For samples with deposited Ni thickness of $\sim 50\text{-}70$ nm and varying poly-Si thickness with $t_{\text{Ni}}/t_{\text{Si}}$ ratios in the ~ 0.6 to 0.9 range and reacted at 450°C , the main phases observed by XRD are NiSi and Ni_2Si (Fig. 1), with NiSi and Ni_2Si as the bottom and top layers respectively as indicated by analysis of the RBS spectra (Fig. 2).

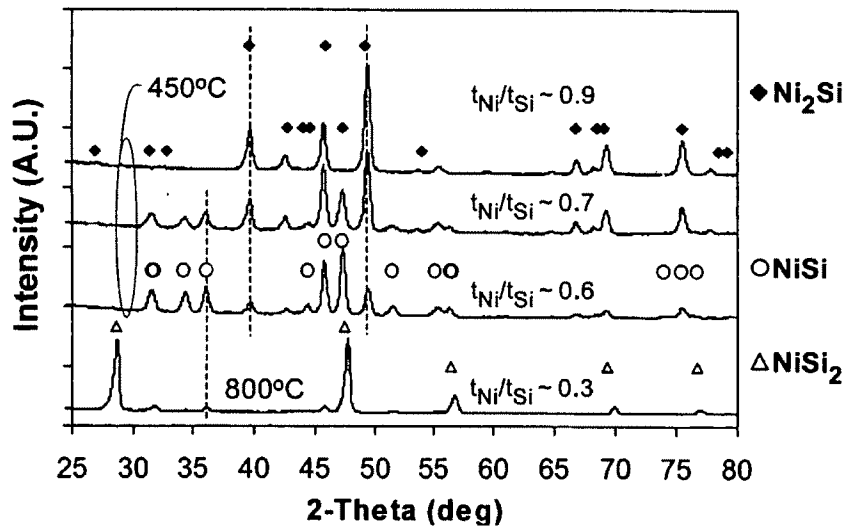


Figure 1. XRD patterns of Ni-silicide on SiO_2 films for deposited Ni to poly-Si thickness ratios ($t_{\text{Ni}}/t_{\text{Si}}$) between 0.3 and 0.9.

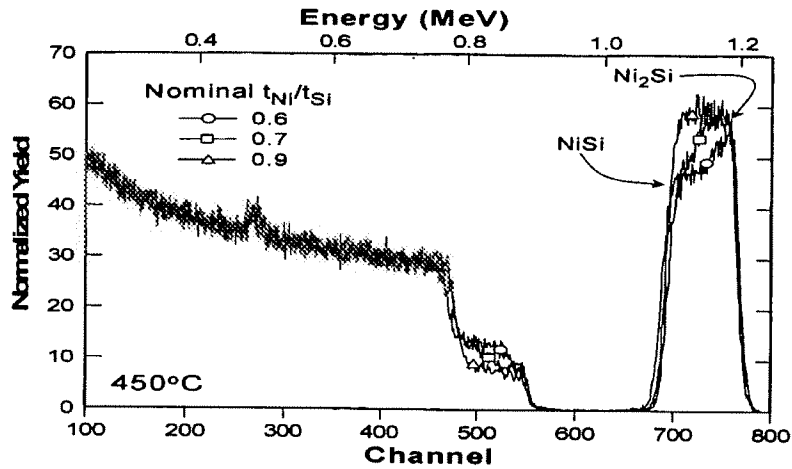
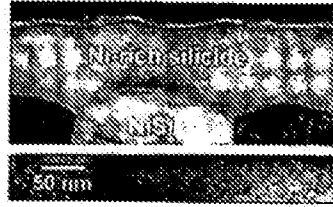


Figure 2. RBS spectra of Ni-silicide on SiO_2 films for deposited Ni to poly-Si thickness ratios ($t_{\text{Ni}}/t_{\text{Si}}$) between 0.6 and 0.9.



5 Figure 3. Cross-section TEM of Ni FUSI gate stack showing bi-layer structure. NiSi was identified in the lower layer by Fourier-transformed high-resolution images. EDX showed a higher Ni/Si composition ratio for the top layer.

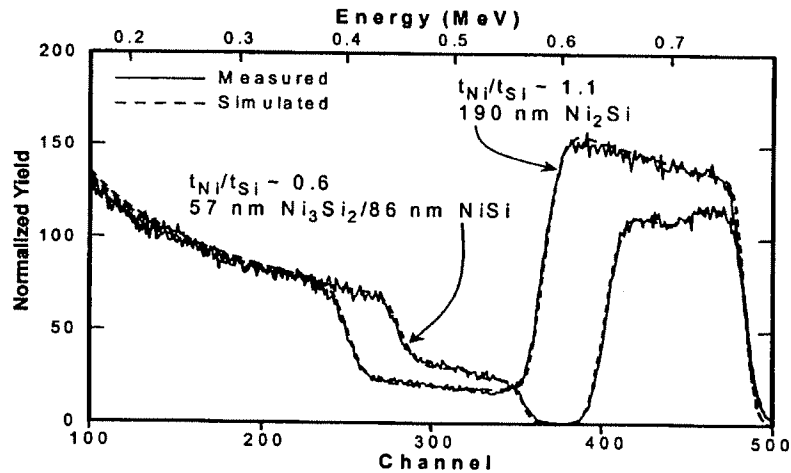


Figure 4. RBS spectra of Ni-silicide on SiO_2 films for deposited Ni to poly-Si thickness ratios ($t_{\text{Ni}}/t_{\text{Si}}$) of 0.6 and 1.1 (1 MeV $^4\text{He}^{++}$, 160°).

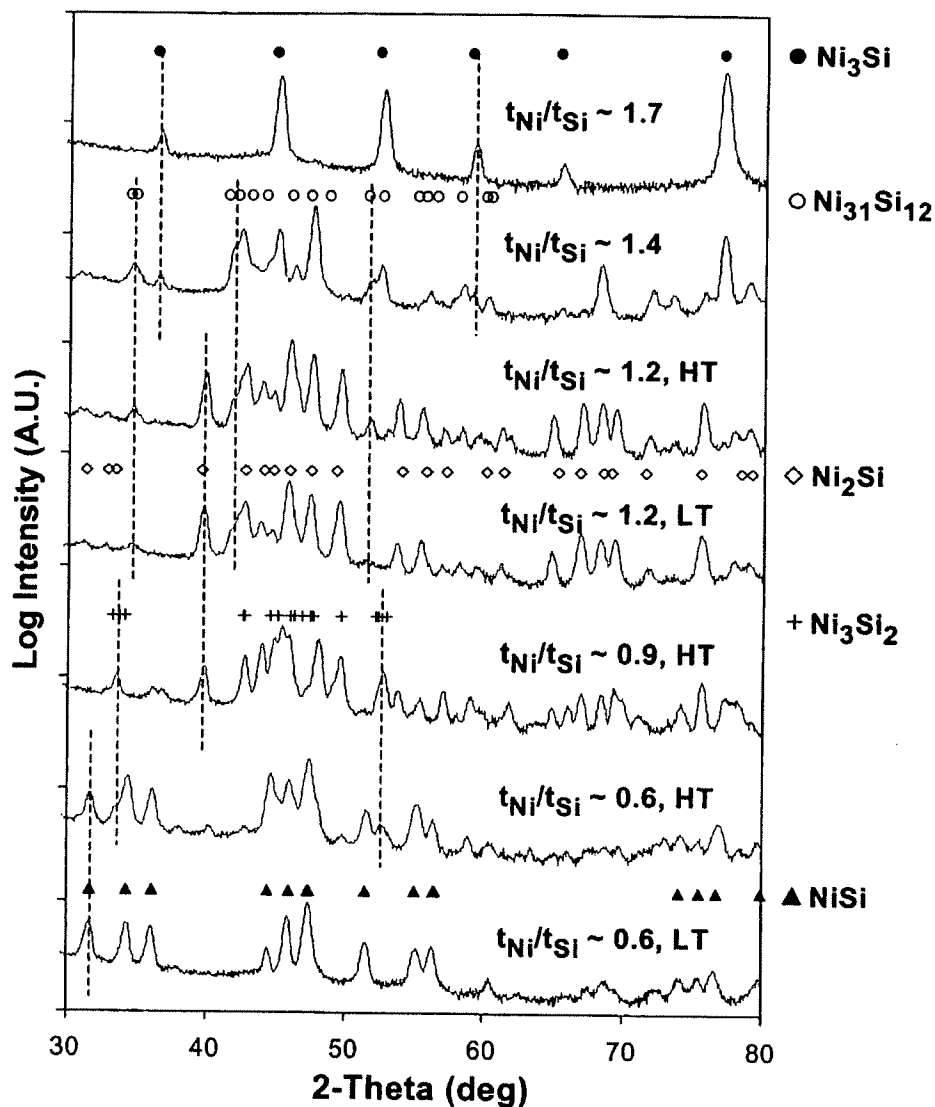


Figure 5. XRD patterns of Ni-silicide on SiO₂ films for deposited Ni to poly-Si thickness ratios ($t_{\text{Ni}}/t_{\text{Si}}$) between 0.6 and 1.7. Results for different silicidation processes are shown for selected thickness ratios (LT and HT indicate lower and higher temperature processes respectively).

Characterization of bi-layer samples with deposited $t_{\text{Ni}}/t_{\text{Si}} \sim 0.6$ by scanning TEM (STEM) energy dispersive X-ray (EDX) analysis was performed for varying processing conditions. The ratio of Ni content (x in Ni_xSi) from the top layer to the bottom layer ($x_{\text{top layer}}/x_{\text{bottom layer}}$) was found to be in the ~ 1.3 to 2 range, suggesting that Ni_3Si_2 and/or Ni_2Si may be present in the top layer, depending on processing conditions. RBS analysis also suggested that a bi-layer structure with Ni_3Si_2 as top layer and NiSi as bottom layer can be obtained (Fig. 4). We note, however, that RBS analysis can only provide information

on the average composition vs. depth, and cannot distinguish between pure phases and phase mixtures. The presence of Ni_3Si_2 as secondary phase was confirmed by XRD analysis of NiSi samples formed from deposited $t_{\text{Ni}}/t_{\text{Si}} \sim 0.6$ by reaction at higher temperatures (HT); see Fig. 5.

- 5 XRD patterns and RBS spectra after silicidation (and selective etch) for samples with deposited $t_{\text{Ni}}/t_{\text{Si}}$ in the 0.6 to 1.7 range (100 nm poly-Si) are shown in Figs. 5 and 6 respectively. As for samples targeting NiSi , a slightly Ni-rich ratio rather than the exact stoichiometric ratio was used for samples targeting the different silicide phases. Fig. 5 shows that Ni-silicide phases with increasing Ni content are observed by XRD as the
- 10 Ni/Si ratio is increased. As $t_{\text{Ni}}/t_{\text{Si}}$ is increased above ~ 0.9 , poly-Si is consumed with formation of Ni-rich silicide phases and NiSi does not form. For $t_{\text{Ni}}/t_{\text{Si}} \sim 0.9$ reacted at higher temperatures (HT), the presence of Ni_3Si_2 and Ni_2Si is observed by XRD (Fig. 5). Ni_2Si films were formed at $t_{\text{Ni}}/t_{\text{Si}} \sim 1.2$ (Figs. 5 and 6). The XRD patterns also indicate the presence of $\text{Ni}_{31}\text{Si}_{12}$ for this thickness ratio, particularly on samples reacted at higher
- 15 temperatures (Fig. 5). The RBS spectra shown in Fig. 6 for $t_{\text{Ni}}/t_{\text{Si}} \sim 1.2$ indicates that the silicide film has a higher Ni content on the top portion and a composition of $\sim \text{Ni}_2\text{Si}$ at the interface, suggesting a layered structure with the Ni-rich phase at the top for this case as well. Samples with a more uniform Ni_2Si composition could also be obtained (Fig. 4). For $t_{\text{Ni}}/t_{\text{Si}} \sim 1.4$, the main phases present as determined from the XRD spectra are $\text{Ni}_{31}\text{Si}_{12}$ and
- 20 Ni_3Si . At $t_{\text{Ni}}/t_{\text{Si}} \sim 1.7$, Ni_3Si films are formed (Figs. 5 and 6), with no indication of second phases in the XRD pattern. For self-aligned FUSI applications, phase control for Ni_3Si is not a significant problem, since this is the Ni-silicide phase with highest Ni content and in consequence it is stable in contact with Ni. Thus, the reaction reaches completion with formation of a uniform Ni_3Si layer and any excess Ni is then removed in the selective
- 25 etch. Ni_3Si is the only phase obtained for reacted Ni to Si thickness ratios > 1.6 .

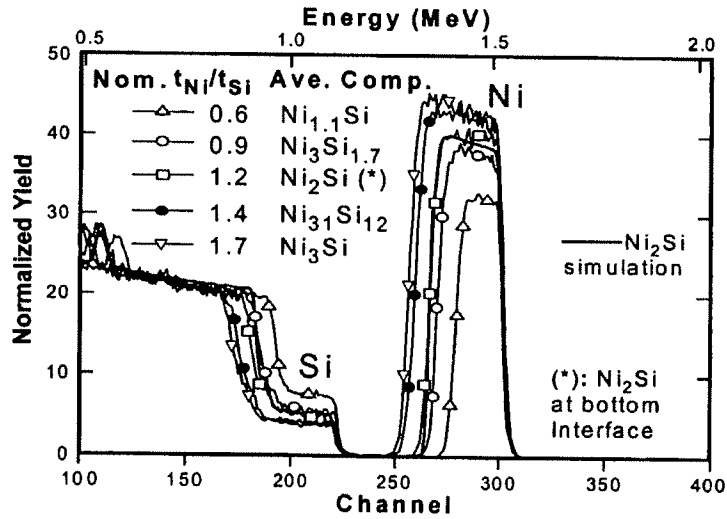


Figure 6. RBS spectra of Ni-silicide on SiO_2 films for deposited Ni to poly-Si thickness ratios ($t_{\text{Ni}}/t_{\text{Si}}$) of 0.6 to 1.7 (2 MeV $^4\text{He}^{++}$, 160°).

Electrical characterization of Ni fully silicided gates

The WF of Ni FUSI gates was extracted from capacitance-voltage (CV) measurements performed on devices for several dielectric EOT values. A dual thickness series with HfSiON/SiO₂ stacks of varying SiO₂ and HfSiON thicknesses was used to evaluate the WF of NiSi on HfSiON, accounting for the effect of bulk charges in HfSiON. Figure 7 shows the dependence of the flat band voltage (V_{fb}) on EOT for NiSi/SiO₂, NiSi/HfSiON/SiO₂ and Ni₂Si/SiO₂ gate stacks, and the effect of dopants. Shifts in WF with dopants (-230 mV for As and +160 mV for B) are seen for NiSi on SiO₂. In contrast, dopant effects on WF are much smaller for NiSi on HfSiON (Fig. 7b). The effective WF values extracted for undoped NiSi were ~4.72 eV on SiO₂ and ~4.5 eV on HfSiON. The lack of significant dopant effects and the WF value observed in this study for NiSi on HfSiON suggest that Fermi level pinning, previously reported for poly-Si gates on Hf containing high-K dielectrics, is still present for NiSi FUSI gates. Fig. 7c shows that the WF of undoped Ni₂Si on SiO₂ (~4.7 eV) is quite similar to that of NiSi on SiO₂. However, in contrast to the case of NiSi, the WF of Ni₂Si on SiO₂ appears not to be affected significantly by the addition of dopants. Fig. 8a shows that for Ni₃Si/SiON, an increase in V_{fb} of ~100 mV from the value for NiSi/SiON is obtained. The change in V_{fb} with silicide phase is quite larger for the case of HfSiON, with an increase of >300 mV from NiSi to Ni₃Si (Fig. 8b), and suggests unpinning of the Fermi level with Ni₃Si.

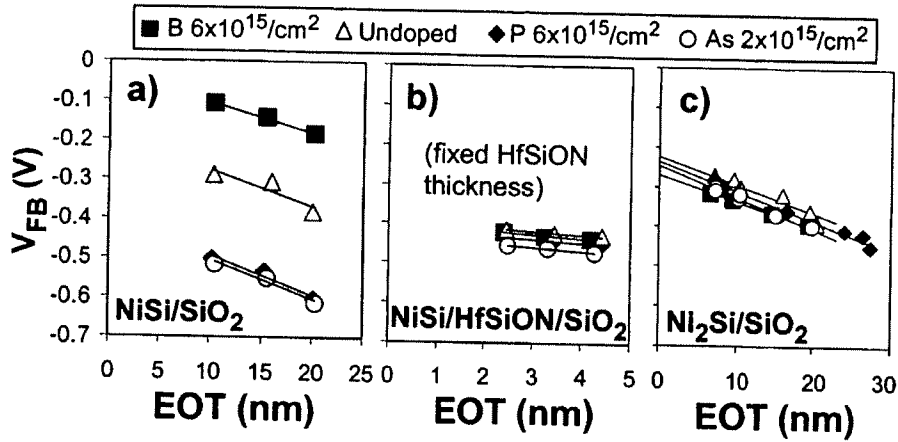


Figure 7. Flat band voltage vs. EOT for a) NiSi/SiO₂, b) NiSi/HfSiON/SiO₂ and c) Ni₂Si/SiO₂ capacitors showing the effect of dopants.

SUMMARY AND CONCLUSIONS

The phases and morphology of Ni FUSI gates were studied for varying Ni to Si thickness ratios. The presence of NiSi₂, NiSi, Ni₃Si₂, Ni₂Si, Ni₃Si₁₂ and Ni₃Si as predominant phases was obtained for increasing Ni to Si ratios. A slightly Ni-rich thickness ratio than that corresponding to stoichiometric NiSi was found suitable for NiSi FUSI gate applications, resulting in a layered structure with NiSi at the interface and a Ni-rich silicide layer on top. No secondary phases were detected on Ni₃Si samples (Ni to Si thickness ratio ~ 1.7). Electrical characterization for NiSi, Ni₂Si and Ni₃Si devices on

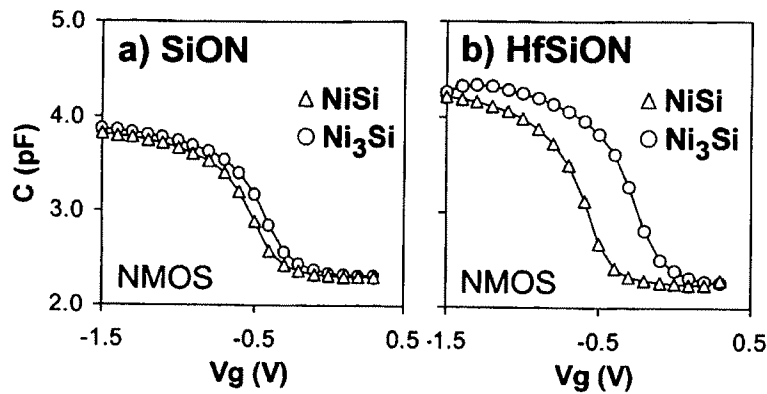


Figure 8. CV curves comparing NiSi and Ni₃Si FUSI gates for a) SiON and b) HfSiON dielectrics.

SiO₂, SiON and high-K dielectrics was performed. Only small changes in flat-band voltage or work function were found between these phases on SiO₂ or SiON for undoped samples. While significant changes in work function with dopants were observed for NiSi on SiO₂, little or no effects were found for NiSi on HfSiON (suggesting Fermi level pinning) and for Ni₂Si on SiO₂. An increase of > 300 mV was found from NiSi to Ni₃Si on HfSiON, suggesting unpinning of the Fermi level with the Ni-rich silicide.

REFERENCES

1. M. Qin, V. M. C. Poon and S. C. H. Ho, *J. Electrochem. Soc.*, **148**, (2001) 271.
2. J. Kedzierski, D. Boyd, P. Ronsheim, S. Zafar, J. Newbury, J. Ott, C. Cabral Jr., M. Jeong and W. Haensch, *IEDM Tech. Dig.*, (2003) 315.
3. J. A. Kittl, A. Lauwers, O. Chamirian, M. A. Pawlak, M. Van Dal, A. Akheyar, M. De Potter, A. Kottantharayil, G. Pourtois, R. Lindsay and K. Maex, *Mater. Res. Soc. Symp. Proc.*, **810**, (2004) 31.
4. K. G. Anil, A. Veloso, S. Kubicek, T. Schram, E. Augendre, J. -F. de Marneffe, K. Devriendt, A. Lauwers, S. Brus, K. Henson and S. Biesemans, *Symp. VLSI Tech. Dig.*, (2004) 190.
5. M. A. Nicolet, S. S. Lau, in N. G. Einspruch and G. B. Larrabee (eds.), *VLSI Electronics: Microstructure Science*, Vol. 6, Ch. 6, Academic Press, New York (1983).
6. C. Lavoie, F. M. d'Heurle, C. Detavernier and C. Cabral Jr., *Microelectronic Engineering*, **70**, (2003) 144.

Scalability of Ni FUSI gate processes: phase and V_t control to 30 nm gate lengths

J. A. Kittl¹, A. Veloso, A. Lauwers, K. G. Anil, C. Demeurisse, S. Kubicek, M. Niwa², M. J. H. van Dal³, O. Richard, M. A. Pawlak, M. Jurczak, C. Vrancken, T. Chiarella, S. Brus, K. Maex and S. Biesemans

IMEC, assignees at IMEC from ¹Texas Instruments and ²Matsushita, ³Philips Research Leuven; Kapeldreef 75, B-3001 Leuven, Belgium, tel.: +32-16-28 1491, Fax +32-16-28 17 06, email: kittl@imec.be

Abstract

We demonstrate for the first time the scalability of NiSi and Ni₃Si FUSI gate processes down to 30 nm gate lengths, with linewidth independent phase and V_t control. We show that 1-step FUSI is inadequate for NiSi FUSI gates, because it results in incomplete silicidation at low thermal budgets or in a linewidth dependent Ni silicide phase –inducing V_t shifts– at higher thermal budgets. We show that V_t and WF shifts are larger on high-K (HfO₂ (250 mV) or HfSiON (330mV)) than on SiON (110mV) and report Fermi level unpinning for Ni-rich FUSI on high-K. In contrast, we demonstrate the scalability of Ni₃Si FUSI, with no phase control issues, and report HfSiON Ni₃Si FUSI PMOS devices with $V_t = -0.33$ V. Lastly, we show that, for NiSi, phase control down to narrow gate lengths can be obtained with a 2-step FUSI process.

Introduction

Ni FUSI gates have recently attracted attention as metal gate candidates for scaled CMOS technologies [1-5]. NiSi [1-4], NiSi₂ and Ni₃Si [5] have been studied as possible gate materials. Due to its high nucleation temperature, NiSi₂ is less attractive for integration into self-aligned FUSI gate processes. The scalability of Ni FUSI gate processes to small gate lengths –critical for advanced CMOS applications– has not yet been addressed in detail, and is the focus of this work.

Experimental

MOSFET devices with Ni FUSI gates (SiON, HfSiON and HfO₂) were fabricated using a self-aligned process with independent silicidation of the source/drain (S/D) and the poly-Si gate using a CMP approach as described in [3,4]. Different Ni/Si ratios were used to obtain the different Ni silicide phases and study their formation as function of gate length. Physical characterization included TEM, SEM, RBS and XRD (RBS and XRD only for blanket films).

Results and Discussion

For blanket Ni films on poly-Si/dielectric stacks, the silicide phase can be effectively controlled by the Ni/Si thickness ratio (t_{Ni}/t_{Si}), when sufficient thermal budgets are used to drive the reaction to completion (Figs. 1, 2). NiSi, Ni₂Si and Ni₃Si phases were found for $t_{Ni}/t_{Si} = 0.6, 1.2$ and 1.7 , respectively (Fig. 1). Since Ni silicides have limited composition range, mixed-phase films are formed between the stoichiometric ratios (with Ni₂Si₂ and Ni₃Si_{1.2} also able to grow at low temperatures). NiSi₂ grows by a nucleation-controlled process and does not form uniformly below 600°C, so that incomplete silicidation is seen for $t_{Ni}/t_{Si} < 0.5$. For $0.6 < t_{Ni}/t_{Si} < 1$, stacks with NiSi at the bottom and Ni-rich silicide layers on top are formed. For $t_{Ni}/t_{Si} > 1.7$ Ni₃Si is the stable phase, and the excess Ni is removed in the selective etch step. The resistivity and thickness of the silicide films increase with increasing Ni/Si ratio (Fig. 2). CV measurements performed on FUSI devices showed larger V_{FB} shifts with change in Ni/Si composition ratio for HfSiON than for SiON (330 and 100 mV respectively, between NiSi and Ni₃Si, Fig. 3). WFs for the most relevant Ni silicide phases are shown in Fig. 4. A significant increase in WF with increasing Ni/Si ratio is observed for HfSiON devices, with only a milder change seen for SiO₂. The difference in NiSi WF observed between HfSiON and SiON, is attributed to Fermi level pinning on high-K devices. This difference disappears for Ni-rich silicides, suggesting the unpinning of the FL.

On patterned devices, the story is quite different. For narrow lines, the Ni/Si ratio is not well defined: Ni from top of spacers and surrounding areas can diffuse and react with poly-Si in the gate to increase the effective Ni/Si ratio (Fig. 5). To understand silicidation of narrow gates, we consider the Ni silicide phase sequence. Ni₂Si grows at low temperatures by Ni diffusion-limited kinetics (Fig. 6), while NiSi growth follows at higher temperatures with same type of kinetics (Fig. 7), only if available Ni is fully consumed and poly-Si is not. If the Ni supply is not limited, the reaction reaches completion with full Ni₃Si silicidation. As a consequence, a FUSI linewidth-

effect is found for conventional 1-step FUSI processes. Using conditions developed for blanket films (60 nm Ni/100 nm poly-Si, 520°C 30s RTP), a transition from full silicidation with NiSi at large gate lengths to full silicidation with Ni-rich silicide at 50 nm gate lengths was found, with the corresponding increase in sheet resistance and silicide thickness (Figs. 8 and 9). The sheet resistance of small gate lengths corresponds to Ni₃Si (Fig. 8). The key negative implication of this is that devices fabricated with this process show kinks in the V_t roll-off characteristics (Figs. 10, 11), consistent with a transition from NiSi to Ni₃Si with decreasing gate length. The kink is of ~250 mV on HfO₂ and of ~110 mV on SiON, consistent with the difference in WF between NiSi and Ni₃Si. The gate lengths at which the transition occurs depends on the thermal budget used (of magnitude of the Ni-rich silicide thickness grown at that thermal budget) and can also depend on details of the geometry (spacer height, etc.). A split of V_t showing a bi-modal distribution that correlates well with R_s values (low V_t -high R_s on PMOS) was observed at the transition gate length. In contrast, for a Ni/Si ratio targeting Ni₃Si ($t_{Ni}/t_{Si}=1.7$), no phase control issues were observed and V_t roll-off characteristics are smooth (Figs. 11, 12). Scalability with good phase and V_t control down to 30 nm gate lengths for Ni₃Si is demonstrated (Fig. 11). PMOS $V_t = -0.33$ V was obtained for Ni₃Si on HfSiON making it an attractive system. V_t values for the $t_{Ni}/t_{Si}=0.6$ 1-step process (NiSi on large structures) and $t_{Ni}/t_{Si}=1.7$ (Ni₃Si) process are seen to merge at small gate lengths (Fig. 11), further confirming the formation of Ni rich silicide at small gate lengths in the 1-step FUSI process.

To solve the linewidth dependence of NiSi FUSI, a 2-step NiSi FUSI process (Fig. 5) was developed. The effective (reacted) Ni/Si ratio is controlled by limiting the RTP1 thermal budget, growing a Ni-rich silicide that does not fully consume the poly-Si thickness. Excess Ni and Ni films on top of spacers/surrounding areas are then removed in the selective etch step. A second RTP step at a higher temperature is then used to grow NiSi, fully siliciding the gates. Fig. 13 shows the effect of RTP1 temperature on sheet resistance of 50 nm and 1000 nm gates for 60nm Ni/100 nm poly-Si, showing the convergence of R_s values with decreasing RTP1 temperature, corresponding to the transition from Ni-rich to NiSi on 50 nm gates. In the 2-step FUSI process, the RTP1 thermal budget needs to be controlled such that the grown Ni₂Si layer has a thickness between 0.9 and 1.5 of the poly-Si thickness, to avoid incomplete silicidation and full silicidation with Ni-rich silicide respectively. The RTP1 process window estimated from Ni₂Si kinetic data (Figs. 6 and 7) is shown in Fig. 14. Margins for process variations and the intrinsic non-uniformity of silicidation need to be taken into account, making the process window ≤ 20 °C. Figs. 8 and 9 show that a 2-step NiSi FUSI process can eliminate the linewidth dependence, allowing the growth of NiSi on large and small structures. Smooth V_t roll-off for the 2-step NiSi FUSI process further confirms that NiSi can be maintained to small gate lengths (Figs. 11, 12).

Conclusions

In this work, for the first time, scalability of NiSi and Ni₃Si FUSI gate processes was demonstrated to 30 nm gate lengths and its underlying mechanisms discussed in detail. For Ni-rich silicides (Ni₂Si), the same WF values (4.8 eV) are observed on SiON and HfSiON, suggesting unpinning of the Fermi level for HfSiON devices. A very attractive $V_t = -0.33$ V is thus obtained for those devices with a scalable process. Smooth V_t roll-off characteristics and elimination of narrow line effect were also shown for a 2-step NiSi FUSI process.

References

- [1] B. Tavel *et al.*, IEDM Tech. Dig., 825 (2001);
- [2] J. Kedzierski *et al.*, IEDM Tech. Dig., 247 (2002), 441 (2003);
- [3] K. G. Anil *et al.*, Symp. VLSI Tech., 190 (2004);
- [4] A. Veloso *et al.*, IEDM Tech. Dig., 855 (2004);
- [5] K. Takahashi *et al.*, IEDM Tech. Dig., 91 (2004)

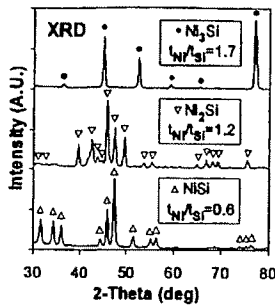


Fig. 1. XRD spectra showing formation of NiSi, Ni₃Si and Ni₂Si by adjusting Ni to Si thickness ratio.

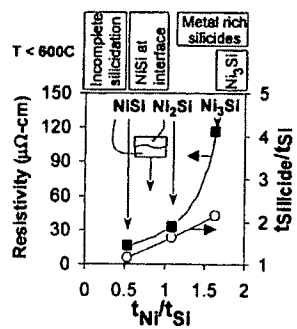


Fig. 2. Increase in resistivity and silicide thickness with increasing Ni to Si thickness ratio.

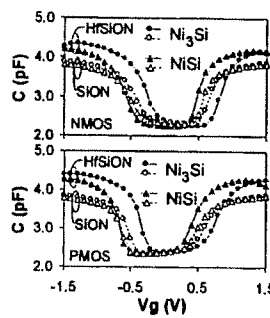


Fig. 3. CV curves for FUSI devices, showing larger V_{FB} shifts from NiSi to Ni₃Si on HfSiON (330 mV) than on SiON (100 mV).

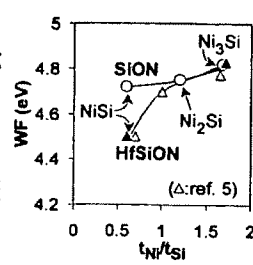


Fig. 4. WF for the main Ni silicide phases. The large difference for NiSi between SiO₂ and HfSiON disappears for larger Ni contents indicating unpinning of the FL.

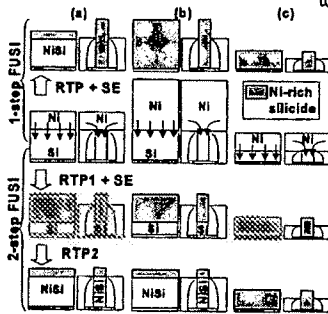


Fig. 5. Schematic showing 1-step and 2-step FUSI processes on wide and narrow gates, for varying Ni and Si thicknesses. Due to Ni diffusion from top of spacers, the effective Ni/Si ratio can be larger for narrow devices than for large structures.

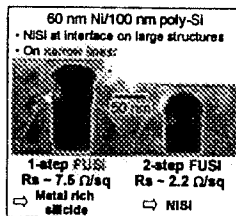


Fig. 9. TEM cross sections of narrow FUSI gates for 1-step and 2-step FUSI processes.

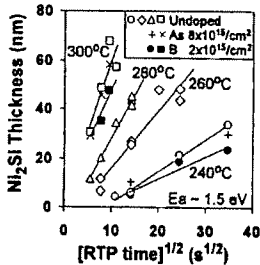


Fig. 6. Ni₂Si silicidation kinetics showing diffusion limited growth.

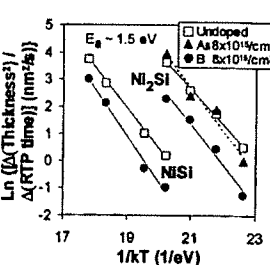


Fig. 7. Silicide growth rates for NiSi and Ni₂Si.

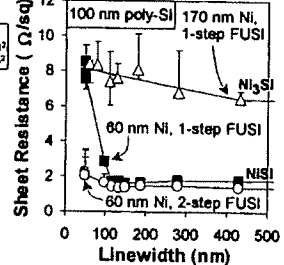


Fig. 8. R_S vs. L showing linewidth effect for 60 nm Ni 1-step FUSI eliminated with 2-step FUSI.

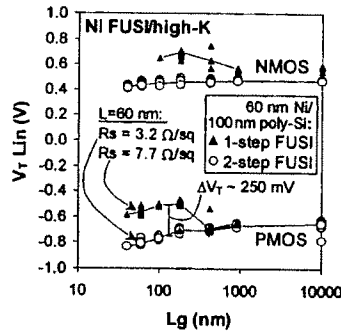


Fig. 10. V_t roll-off for 1-step and 2-step Ni FUSI/HfO₂ processes. The kink seen for the 1-step process is due to transition from NiSi for long gate lengths to Ni-rich silicide on short ones.

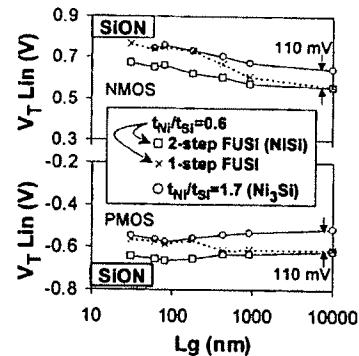


Fig. 11. V_t roll-off for Ni FUSI/SiON processes. For $t_{Ni}/t_{Si}=0.6$ (targeting NiSi), the 1-step process shows a kink corresponding to the transition from NiSi at long gate lengths to Ni-rich silicide at short gate lengths. Ni₃Si and 2-step NiSi FUSI processes show smooth V_t roll-off to 30 nm gate lengths.

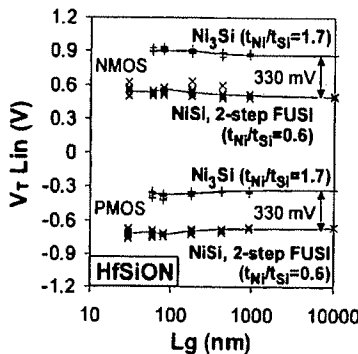


Fig. 12. V_t roll-off for Ni FUSI/HfSiON showing scalability with smooth roll-off for Ni₃Si and 2-step NiSi FUSI processes.

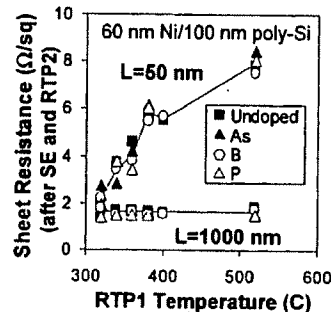


Fig. 13. R_S vs. RTP1 temperature for 2-step Ni FUSI process. The increase in R_S with increasing temperature for 50 nm gates is due to the transition from NiSi to Ni-rich silicide.

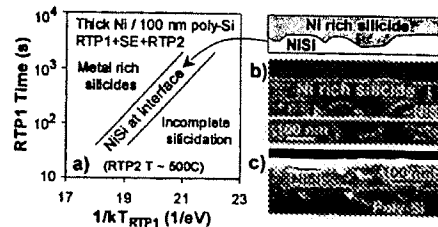


Fig. 14. a) RTP1 process window for 2-step NiSi FUSI process. Process margins need to be added to account for process variations and silicide reaction non-uniformity (b and c).

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☒ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☒ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.